FROM THE EDITOR-IN-CHIEF

Computing With COOL Chips

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Warm greetings for the new year! This is Hsien-Hsin Sean Lee. I am thrilled to assume the esteemed role of editor-in-chief of *IEEE Micro*, succeeding Prof. Lizy John, starting January 2024. It is a great honor and privilege to have the opportunity to serve and contribute to the computer architecture and system community through this prestigious publication venue. I look forward to all readers' support and assistance to help uphold and carry forward the legacy of this magazine. My commitment is to continue delivering to you the latest research and technical outcomes from not only computer architecture but also their interdisciplinary innovations from both academia and industry. Today, research, technology development, and product deployment are going through a transformative Cambrian era. Tight-knit co-design and co-optimization among emerging applications [e.g., AI/machine learning (ML)], software, and hardware are becoming indispensable for delivering optimal, high-efficiency solutions. I envision *IEEE Micro* playing a pivotal role in this interesting time.

Driven by the ever-increasing demand for computing power with the relentless development advancement of modern workloads, such as AI/ML designed with novel technologies, minimizing energy consumption for each operation—irrespective of whether it is computation or memory access—has become the first-class design objective across all design fronts. Keeping the chips' operations cool not only lowers the total cost of ownership but also makes them scalable and minimizes the impact to the environment.

For this Special Issue on COOL Chips, I would like to thank Prof. Ryusuke Egawa from Tokyo Denki University and Prof. Yasutaka Wada from Meisei University for serving as the guest coeditors and coordinating the entire review process. Four papers, originally published at the IEEE Symposium on Low-Power and High-Seed Chips and Systems (COOL Chips Conference), were selected and extended for inclusion in this special issue. Among these works, three articles specifically aim at bringing low-power techniques to various neural network architectures, including spiking neural network (SNN) and deep neural network (DNN), without compromising the quality of the ML models used in their studies. One article discusses a new integrity verification technique to address the energy efficiency challenges in prior integrity check schemes using a cache Merkle tree for secure nonvolatile memory systems. Refer to the guest editorial by Prof. Egawa and Prof. Wada[A1] for the preview of these four articles.

In addition, we include two general technical articles in this issue. The first article is "Privacy by Memory Design: Visions and Open Problems,"[A2] by Liu and Gong from North Carolina State University and the University of South Alabama. The authors introduce a prototype architecture design to achieve differential privacy at low power on a 45-nm customized static random-access memory chip. The second article, "Acceleration of a Classic McEliece Postquantum

APPENDIX: RELATED ARTICLES

A1. R. Egawa and Y. Wada, "Special Issue on COOL Chips," *IEEE Micro*, vol. 44, no. 1, pp. 6–7, Jan./Feb. 2024, doi: 10.1109/MM.2024.3353949.

A2. J. Liu and N. Gong, "Privacy by memory design: Visions and open problems," *IEEE Micro*, vol. 44, no. 1, pp. 49–58, Jan./Feb. 2024, doi: 10.1109/MM.2023.3337094.

A3. C. Nugier and V. Migliore, "Acceleration of a classic McEliece postquantum cryptosystem with cache processing," *IEEE Micro*, vol. 44, no. 1, pp. 59–68, Jan./Feb. 2024, doi: 10.1109/MM.2023.3304425.

A4. J. J. Yi, "Analysis of historical patenting behavior and patent characteristics of computer architecture companies—Part VIII: Patent families," *IEEE Micro*, vol. 44, no. 1, pp. 70–74, Jan./Feb. 2024, doi: 10.1109/MM.2024.3353948.

A5. S. Greenstein, "After the gold rush," *IEEE Micro*, vol. 44, no. 1, pp. 75–77, Jan./Feb. 2024, doi: 10.1109/MM.2023.3339186.

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Cryptosystem With Cache Processing,"[A3] by Nugier and Migliore from Institut National des Sciences Appliquées de Toulouse (INSA-Toulouse), demonstrates a design that achieves substantial performance improvement on hardware systems supporting processing-in-memory technology for the classic McEliece key encapsulation mechanism for postquantum cryptography. Both articles are eminent demonstrations of interdisciplinary research outcomes, offering effective architectural solutions and insights for emerging areas in security and privacy as well as postquantum cryptography.

These articles are followed by a Micro Law department article by Yi.[A4] This is part of Yi's article series on his characterization and analysis of patents related to computer architecture versus all other patents filed by companies designing semiconductor chips and computing systems. In the article of the current issue, Yi analyzes the characteristics and ratios of issued patents in different patent families for 18 companies between 1996 and 2020. Understanding these ratios sheds light on the significance of the inventions in a patent family for a company. In addition, Greenstein of Harvard Business School contributes a Micro Economics department article.[A5] In "After the Gold Rush," Greenstein discusses the commercial risks arising from our limited understanding of generative AI when this technology is rapidly adopted and deployed to the general public. He further explores how corporations can manage these risks through different strategies to reduce hallucinations and minimize potential detriments to their business.

I hope you enjoy the articles we selected for you in this issue and wish you all a productive and prosperous 2024.

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