Hsien-Hsin Sean Lee, Ph.D.

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Intel Fellow | Editor-in-Chief, IEEE MICRO | IEEE Fellow

PROFESSIONAL PROFILE

Distinguished technology executive and computer architect with over 30 years of leadership across computer architecture, system software, semiconductors, and AI. Currently as an *Intel Fellow*, leads GPU and AI infrastructure pathfinding and product incubation for Intel's Data Center Group. Draws on extensive experience in both academia (Georgia Tech) and industry (Intel, TSMC, and Meta), with a proven track record of building and scaling world-class global RD organizations.

PROFESSIONAL EXPERIENCE

Intel Corporation Hudson, MA
Intel Fellow (Technology VP), AI System Architecture, Datacenter Group Aug 2022 – Present

- Drive AI infrastructure technology pathfinding and product incubation.
- Lead CPU/GPU performance methodology and corporate strategy for AI workloads.
- Lead confidential AI and software stack strategy.
- Lead dynamic auto-tuning optimization frameworks.
- Key architect pushing architecture and emerging technology for datacenter GPU products.

Meta / Facebook, Inc. Cambridge, MA
Area Research Lead, Facebook AI Research (FAIR) March 2020 – Aug 2022
Research Head, AI Infrastructure Research Jan 2019 – Feb 2020

- Established the "Systems for ML" research group from inception at the Facebook Boston site.
- Led R&D in high-efficiency personalized recommendation system designs.
- Led prototyping of processing-near-memory and emerging memory technology for AI workloads.
- Led research in sustainable, carbon-aware computing for machine learning.
- Led R&D for privacy-preserving machine learning.

Taiwan Semiconductor Manufacturing Company (TSMC) Hsinchu, Taiwan
Deputy Director, Design Methodology and Kits Development Division Apr 2012 – Jan 2019

- Directed 6 departments and 155 R&D staff across Taiwan, China, and the US developing IC design methodology, EDA tool features, and PDK for all TSMC customers for all nodes.
- Led IC design ecosystem enablement across TSMC, EDA vendors, and fabless design companies.
- Technology owner for all design collateral incl. advanced packaging (CoWoS, SoIC, WoW).
- Technology owner of machine learning applications for quality of physical verification.

Georgia Institute of Technology Atlanta, GA
Associate Professor (Tenured), School of ECE July 2008 – June 2014
Assistant Professor, School of ECE July 2002 – June 2008

- Research program spanned multicore architecture, 3DIC, emerging memory technology, green datacenters, secure architecture, FPGA.
- Secured over $5.8M (my own portion) in federal and industry funding.

Agere Systems Atlanta, GA
Architecture Manager, StarCore DSP Technology Center July 2001 – Aug 2002

- Managed 10 DSP architects from Agere and Motorola.
- Led StarCore DSP architecture development for 3G infrastructure.

Intel Corporation Santa Clara / Folsom, CA
Senior Processor Architect / Microprocessor Research Labs Researcher Oct 1995 – July 2001

- Pathfinding for next-gen IA64/EPIC architecture.
- Processor Architect of Pentium-III and Timna (early prototype of integrated CPU/GPU).
- Pentium III post-silicon validation.
- Coded and optimized Microsoft Direct3D 6.1 API using SSE ISA (assembly).

EDUCATION

Massachusetts Institute of Technology (MIT) Cambridge, MA
Executive MBA, Sloan School of Management Expected 2026
University of Michigan Ann Arbor, MI
Ph.D. in Computer Science and Engineering 2001
- Recipient of the Horace H. Rackham Distinguished Dissertation Award.
- Nominated by University of Michigan for ACM Doctoral Thesis Award.

M.S.E. in Computer Science and Engineering 1994
National Tsing-Hua University Hsinchu, Taiwan
B.S. in Electrical Engineering (Valedictorian of Class 1990) 1990

HONORS, SCHOLARSHIP, & SERVICES

- **IEEE Fellow:** Class of 2017, for contributions to 3D-ICs and Computer Architecture.
- **Hall of Fame:** Inducted into the MICRO and HPCA Halls of Fame.
- **Scholarly Impact:** Published 147 peer-reviewed papers; holder of 45 issued US Patents.
- **Awards:** 10-year Most Significant Paper (ITC 2017), NSF CAREER Award (2007), DoE CAREER Award (2005), and 3-time Top Picks papers in Computer Architecture (IEEE MICRO).
- **Editor-in-Chief:** IEEE MICRO (2024 – Present).
- **Program Chairs:** MICRO 2016, ISCA Industry Track 2021, SEED 2022.
- **General Chair:** IISWC 2010.

NOTABLE STUDENTS SUPERVISED AT GEORGIA TECH

- **Josh Fryman, Ph.D.** CTO & Fellow, Intel Government Technology, Intel Corp., OR.
- **Weidong (Larry) Shi, Ph.D.** Associate Professor, CS department, University of Houston, TX.
- **Taeweon Suh, Ph.D.** Professor, CSE department, Korea University, Seoul, South Korea.
- **Chinnakrishnan Ballapuram. Ph.D.** Sr. Director & HBF Base Die Chief Architect, Sandisk, CA.
- **Dong Hyuk Woo, Ph.D.** Sr. VP of AGI, Samsung, CA.
- **Mrinmoy Ghosh, Ph.D.** Sr. Director, HW/SW Co-Design, Samsung, CA.
- **Nak Hee Seong, Ph.D.** VP & Head of SOC IP Development, Samsung, South Korea.
- **Fayez Mohamood, M.S.** Founder and CEO of Bluecore (a unicorn startup), NY.
- **Richard Yoo, M.S.** CTO, Lunit, Seoul, South Korea.
- **Ilya (Khorosh) Tillis, B.S./M.S.** VP, Codility.
- **Greg Diamos, B.S.** Distinguished AI Engineer of multiple AI startups, CA.
- **June Paik (Joonho Baek), B.S.** Founder and CEO of Furiosa AI, South Korea/USA.

KEYNOTE SPEECH HIGHLIGHTS

- **Plenary Speaker.** "Technological Challenges of Social Network Computing" in International Conference on Electronics, Information, and Communication, Jeju, Korea, 2022.
- **Keynote Speaker.** "Challenges of Modern Computing on Social Network Platform" in Research Summit at the Center for Unstoppable Computing, University of Chicago, 2021.
- **NSF Keynote Speaker.** "When Memory Meets ML on Social Network Platform" in NSF Workshop on Processing-In-Memory Technology, National Science Foundation, 2021.
- **ECE Distinguished Lecture Series.** "Machine Learning on Social Network Platform" in George Washington University, Washington D.C., 2020.
- **CASPA Keynote Speaker.** "The Computing Frontiers of Social Network" in Chinese American Semiconductor Professional Association (CASPA) 2019 Annual Conference, Fremont, CA, 2019.
- **ISPLED Keynote Speaker.** "The Computing Frontiers of Social Network" in ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED-2019), Lausanne Switzerland, 2019.
- **ISSCC Forum Speaker.** "Ecosystem of Design for Security" in Design Forum of the International Solid-State Circuits Conference (ISSCC-2016), CA, 2016.
- **Distinguished Speaker.** "3D Integration" in the Computer Information Science Engineering Department Colloquium, University of Florida, Gainesville, FL, 2010.

PATENTS

I hold **45 US issued patents** in the areas of machine learning, memory subsystem, secure non-volatile memory, 3D-IC, and physical design.

BOOK CHAPTERS

BK1. Sungkap Yeo and Hsien-Hsin S. Lee. "Peeling the Power Onion of Data Centers." Chapter Three In Energy Efficient Thermal Management of Data Centers by Yogendra Joshi and Pramod Kumar (Editors), pp.137-168, Springer, 2012.

BK2. Abderrahim Benquassmi, Eric Fontaine, and Hsien-Hsin S. Lee. "Parallelization of Katsevich CT Image Reconstruction Algorithm on Generic Multi-Core Processors and GPGPU." In GPU Computing GEMS, Section 10 Medical Imaging, Chapter 31, Wen-Mei Hwu (editor-in-chief), pp.659-677, Morgan Kaufmann Publishers, 2011.

BK3. Intel 64 and IA-32 Architectures Optimization Reference Manual. (I was the original author of the Chapter of *Optimizing Cache Usage.*

JOURNAL & CONFERENCE PUBLICATION (BY AREAS)

Machine Learning Systems

ML1. Wenjie Xiong, Liu Ke, Maxim Ostapenko, Yongmin Tai, Yeongon Cho, Joonho Song, Jinin So, Kyungsoo Kim, Yongsuk Kwon, Jin Jung, Jieun Lee, Byeongho Kim, Shin-haeng Kang, Sukhan Lee, Jeonghyeon Cho, Kyomin Sohn, Xuan Zhang, Hsien-Hsin S. Lee, G. Edward Suh. "Accelerating Confidential Recommendation Model Inference with Near-Memory Processing." In IEEE Transactions on Dependable and Secure Computing, Vol 22, Issue 4, pg.3580-3586, 2025.

ML2. Haiyang Huang, Newsha Ardalani, Anna Sun, Liu Ke, Shruti Bhosale, Hsien-Hsin S. Lee, Carole-Jean Wu, Benjamin C. Lee. "Toward Efficient Inference for Mixtures of Experts." In the *38th Annual Conference on Neural Information Processing System (NeurIPS'24)*, Vancouver, Canada, December 2024.

ML3. Trishita Tiwari, Suchin Gururangan, Chuan Guo, Weizhe Hua, Sanjay Kariyappa, Udit Gupta, Wenjie Xiong, Kiwan Maeng, Hsien-Hsin S. Lee, G. Edward Suh. "Information Flow Control in Machine Learning Through Modular Model Architecture." In the *33rd USENIX Security Symposium*, Philadelphia, PA, August, 2024.

ML4. Maximilian Lam, Jeff Johnson, Wenjie Xiong, Kiwan Maeng, Udit Gupta, Yang Li, Liangzhen Lai, Ilias Leontiadis, Minsoo Rhu, Hsien-Hsin S. Lee, Vijay Janapa Reddi, Gu-Yeon Wei, David Brooks, G. Edward Suh. "GPU-based Private Information Retrieval for On-Device Machine Learning." In the *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-2024)*, San Diego, California, April, 2024.

ML5. Vivek Parmer, Syed Shakib Sarwar, Ziyun Li, Hsien-Hsin S. Lee, Barbara De Salvo, Manan Suri. "Exploring Memory-Oriented Design Optimization of Edge-AI Hardware for Extended Reality Applications." In *IEEE MICRO Special Issue on TinyML*, Volume 43, Issue 6, 2023.

ML6. Sanjay Kariyappa, Chuan Guo, Kiwan Maeng, Wenjie Xiong, Edward Suh, Moinuddin K. Qureshi, and Hsien-Hsin S. Lee. "Cocktail Party Attack: Breaking Aggregation-based Privacy in Federated Learning Using Independent Component Analysis." In the *40th International Conference on Machine Learning (ICML'2023)*, Honolulu, Hawaii, July, 2023.

ML7. Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, Carole-Jean Wu. "Architectural CO_2 Footprint Tool: Designing Sustainable Computer Systems With an Architectural Carbon Modeling Tool." In *IEEE MICRO special issue on Top Picks from the Computer Architecture Conferences of 2022*, Volume 43, Issue 4, pp.107-117, 2023.

ML8. Vivek Parmer, Syed Shakib Sarwar, Ziyun Li, Hsien-Hsin S. Lee, Barbara De Salvo, Manan Suri. "Memory-Oriented Design Space Exploration of Edge-AI Hardware for XR Applications." In tinyML Research Symposium (tinyML-2023), 2023.

ML9. Jiaxun Cui, Xiaomeng Yang, Mulong Luo, Geunbae Lee, Peter Stone, Hsien-Hsin S. Lee, Benjamin Lee, G. Edward Suh, Wenjie Xiong, Yuandong Tian. "MACTA: A Multi-agent Reinforcement Learning Approach for Cache Timing Attacks and Detection." In the *11th International Conference on Learning Representations (ICLR-2023)*, Kigali, Rwanda, May, 2023.

ML10. Mulong Luo, Wenjie Xiong, Geunbae Lee, Yueying Li, Xiaomeng Yang, Amy Zhang, Yuandong Tian, Hsien-Hsin S. Lee, G. Edward Suh. "AutoCAT: Reinforcement Learning for Automated Exploration of Cache Timing-Channel Attacks." In *Proceedings of the 29th IEEE International Symposium on High-Performance Computer Architecture (HPCA-29)*, Montreal, QC, Canada, Feb, 2023.

ML11. Hanieh Hashemi, Wenjie Xiong, Liu Ke, Kiwan Maeng, Murali Annavaram, G. Edward Suh, and Hsien-Hsin S. Lee. "Private Data Leakage via Exploiting Access Patterns of Sparse Features in Deep Learning-based Recommendation Systems." In the *2022 Trust and Socially Responsible Machine Learning* co-located with *NeurIPS*, December, 2022.

ML12. Carole-Jean Wu, Ramya Raghavendra, Udit Gupta, Bilge Acun, Newsha Ardalani, Kiwan Maeng, Gloria Chang, Fiona Aga, James Huang, Charles Bai, Michael Gschwind, Anurag Gupta, Myle Ott, Anastasia Melnikov, David Brooks, Geeta Chauhan, Benjamin Lee, Hsien-Hsin S. Lee, Bugra Akyildiz, Maximilian Balandat, Joe Spisak, Ravi Jain, Mike Rabbat, Kim Hazelwood. "Sustainable AI: Environmental Implications, Challenges, and Opportunities." In the *Fifth Conference on Machine Learning and Systems (MLSys)*, August, 2022.

ML13. Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. "ACT: Designing Sustainable Computer Systems with an Architectural Carbon Footprint Modeling Tool." In *Proceedings of the 49th ACM/IEEE International Symposium on Computer Architecture (ISCA-49)*, pp.784-799, New York, New York, June, 2022.

ML14. Yongqin Wang, Edward Suh, Wenjie Xiong, Benjamin Lefaudeux, Brian Knot, Murali Annavaram, and Hsien-Hsin S. Lee. "Characterization of MPC-based Private Inferences for Transformer-based Models." In *2022 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2022)*, pp.187-197, May, 2022.

ML15. Udit Gupta, Young Geun Kim, Sylvia Lee, Jordan Tse, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks, Carole-Jean Wu. "Chasing Carbon: The Elusive Environmental Footprint of Computing." In *IEEE MICRO Top Picks from 2021 Computer Architecture Conferences*, pp.37-47, July-Aug, 2022.

ML16. Wenjie Xiong, Liu Ke, Dimitrije Jankov, Michael Kounavis, Xiaochen Wang, Eric Northup, Jie Amy Yang, Bilge Acun, Carole-Jean Wu, Ping Tak Peter Tang, G. Edward Suh, Xuan Zhang, and Hsien-Hsin S. Lee. "SecNDP: Secure Near-Data Processing with Untrusted Memory." In *the 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA-28)*, pp. 244-258, Seoul, South Korea, April, 2022.

ML17. Liu Ke, Udit Gupta, Mark Hempstead, Carole-Jean Wu, Hsien-Hsin S. Lee, and Xuan Zhang. "Hercules: Heterogeneity-aware Inference Serving for At-scale Personalized Recommendation." In *the 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA-28)*, pp. 141-154, Seoul, South Korea, April, 2022.

ML18. Liu Ke, Xuan Zhang, Jinin So, Jong-Geon Lee, Shin-Haeng Kang, Sukhan Lee, Songyi Han, Yeongon Cho, Jin Hyun Kim, Yongsuk Kwon, Kyungsoo Kim, Jin Jung, Ilkwon Yun, Sung Joo Park, Hyunsun Park, Joonho Song, Jeonghyeon Cho, Kyomin Sohn, Nam Sung Kim, and Hsien-Hsin S. Lee. "Near-Memory Processing in Action: Accelerating Personalized Recommendation with AxDIMM." In *IEEE MICRO Special Issue on Processing-In-Memory*, January/February, 2022.

ML19. Udit Gupta, Samuel Hsia, Jeff Zhang, Mark Wilkening, Javin Pombra, Hsien-Hsin S. Lee, Gu-Yeon Wei, Carole-Jean Wu, and David Brooks. "RecPipe: o-designing Models and Hardware to Jointly Optimize Recommendation Quality and Performance." In *Proceedings of the 54th ACM/IEEE International Symposium on Microarchitecture (MICRO-54)*, pp.870-884, Athens, Greece, October, 2021.

ML20. Brandon Reagen, Woo-Seok Choi, Yeongil Ko, Vincent T. Lee, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks. "Cheetah: Optimizing and Accelerating Homomorphic Encryption for Private Inference." In *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA-27)*, Seoul, South Korea, February, 2021.

ML21. Udit Gupta, Young Geun Kim, Sylvia Lee, Jordan Tse, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks, Carole-Jean Wu. "Chasing Carbon: The Elusive Environmental Footprint of Computing." In *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA-27)*, Seoul, South Korea, February, 2021.

ML22. Udit Gupta, Samuel Hsia, Vikram Saraph, Xiaodong Wang, Brandon Reagen, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. "DeepRecSys: A System for Optimizing End-to-End At-Scale Neural Recommendation Inference." In *Proceedings of the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA-47)*, Valencia, Spain, 2020.

ML23. Liu Ke, Udit Gupta, Carole-Jean Wu, Benjamin Cho, Mark Hempstead, Brandon Reagen, Xuan Zhang, David Brooks, Vikas Chandra, Utku Diril, Amin Firoozshahian, Bill Jia, Kim Hazelwood, Hsien-Hsin S. Lee, Meng Li, Bert Maher, Dheevatsa Mudigere, Maxim Naumov, Martin Scharz, Mikhail Smelyanksiy, an Xiaodong Wang. "RecNMP: Accelerating Personalized Recommendation with Near-Memory Processing." In *Proceedings of the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA-47)*, Valencia, Spain, 2020.

ML24. Udit Gupta, Carole-Jean Wu, Xiaodong Wang, Maxim Naumov, Brandon Reagen, David Brooks, Bradford Cottel, Kim Hazelwood, Mark Hempstead, Bill Jia, Hsien-Hsin S. Lee, Andrey Malevich, Dheevatsa Mudigere, Mikhail Smelyanskiy, Liang Xiong, and Xuan Zhang, "The Architectural Implications of Facebook's DNN-based Personalized Recommendation." In *Proceedings of the 26th IEEE International Symposium on High-Performance Computer Architecture (HPCA-26)*, San Diego, CA, February, 2020.

ML25. Lifeng Nai, Yinglong Xia, Ching-Yung Lin, Bo Hong, and Hsien-Hsin S. Lee. "Cache-conscious Graph Collaborative Filtering on Multi-socket Multicore Systems". In *Proceedings of the 11th ACM Conference on Computing Frontiers*, Article No. 32, Cagliari, Italy, 2014.

ML26. Richard M. Yoo, Han Lee, Kingsum Chow, and Hsien-Hsin S. Lee, "Constructing a Non-Linear Model with Neural Networks For Workload Characterization." In *Proceedings of the 2006 IEEE International Symposium on Workload Characterization (IISWC-06)*, pp.150-159, San Jose, California, October, 2006.

Datacenter, Cloud, and Multi-core Computing

DC1. Sungkap Yeo, Mohammad M. Hossain, Jen-Cheng Huang, and Hsien-Hsin S. Lee. "ATAC: Ambient Temperature-Aware Capping for Power Efficient Datacenters." In *Proceedings of the ACM Symposium on Cloud Computing*, pp.17.1-17.14, Seattle, WA, 2014.

DC2. Sungkap Yeo and Hsien-Hsin S. Lee. "Peeling the Power Onion of Data Centers." Chapter Three In *Energy Efficient Thermal Management of Data Centers* by Yogendra Joshi and Pramod Kumar (Editors), pp.137-168, Springer, 2012.

DC3. Mohammad M. Hossain, Jen-Cheng Huang, and Hsien-Hsin S. Lee. "Migration Energy-Aware Workload Consolidation in Enterprise Clouds." In *Proceedings of?the IEEE International Conference on Cloud Computing Technology and Science*, pp.405-410, December, 2012.

DC4. Sungkap Yeo and Hsien-Hsin S. Lee. "SimWare: A Holistic Warehouse-scale Computer Simulator." In *IEEE Computer Special Issue on Modeling and Simulation of Smart and Green Computing Systems*, Vol. 35, No. 9, pp.48-55, 2012.

DC5. Sungkap Yeo and Hsien-Hsin S. Lee. "Using Mathematical Modeling in Provisioning a Heterogeneous Cloud Computing Environment." In *IEEE Computer*, Vol. 44, No. 8, pp. 55-62, August, 2011.

DC6. Mrinmoy Ghosh, Ripal Nathuji, Min Lee, Karsten Schwan, and Hsien-Hsin S. Lee. "Symbiotic Scheduling for Shared Caches in Multi-Core Systems Using Memory Footprint Signature." In *Proceedings of the 40th IEEE International Conference on Parallel Processing (ICPP-2011)*, Taipei, Taiwan, pp.11 - 20, September, 2011. (Acceptance rate = 22%, 81/363)

DC7. Sung Woo Chung, Hsien-Hsin S. Lee, and Woo Hyong Lee. "Architecture/OS Support for Embedded Multi-core Systems." In *The Computer Journal*, vol.53, no.8, pp.1134-1135, 2010.

DC8. Dong Hyuk Woo and Hsien-Hsin S. Lee. "PROPHET: Goal-Oriented Provisioning for Highly Tunable Multicore Processors in Cloud Computing." In *ACM SIGOPS Operating Systems Review special issue on the Interaction among the OS, Compilers, and Multicore Processors*, Vol.43, Issue 2, pp.102-103, April, 2009.

DC9. Michael Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, and Sung Kyu Lim. "Thermal optimization in Multigranularity Multi-Core Floorplanning." In *Proceedings of the 14th IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC'09)*, pp.43-48, Yokohama, Japan, January, 2009.

DC10. Dong Hyuk Woo and Hsien-Hsin S. Lee. "Extending Amdahl's Law for Energy-Efficient Computing in the Many-Core Era." In *IEEE Computer*, Vol.41, No.12, pp.24-31, December, 2008.

DC11. Richard M. Yoo and Hsien-Hsin S. Lee, "Adaptive Transaction Scheduling for Transactional Memory Systems." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp. 169-178, Munich, Germany, 2008.

DC12. Richard M. Yoo, Yang Ni, Adam Welc, Bratin Saha, Ali-Reza Adl-Tabatabai, and Hsien-Hsin S. Lee, "Kicking the Tires of Software Transactional Memory: Why the Going Gets Tough." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp.265-274, Munich, Germany, 2008.

DC13. Richard M. Yoo and Hsien-Hsin S. Lee. "Helper Transactions: Enabling Thread-Level Speculation via A Transactional Memory System." In *Workshop on Parallel Execution of Sequential Programs on Multicore Architectures (PESPMA) in Conjunction with ACM/IEEE International Symposium on Computer Architecture (ISCA-35)*, Beijing, China, June 2008.

DC14. Taeweon Suh, Daehyun Kim, and Hsien-Hsin S. Lee, "Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MP SoCs." In *Proceedings of the 42nd Design Automation Conference (DAC-42)*, pp.553-558, Anaheim, California, June 2005. (acceptance rate=20%)

DC15. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 2." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.70-78, September/October 2004.

DC16. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 1." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.33-41, July/August 2004.

DC17. Taeweon Suh, Douglas M. Blough and Hsien-Hsin S. Lee, "Supporting Cache Coherence in Heterogeneous Multiprocessor Systems." In *Proceedings of the Design Automation and Test in Europe Conference (DATE'04)*, pp.1150-1155, Paris, France, February 2004. (acceptance rate = 23.2%, 181/780)

GPU and Heterogeneous Architecture

GP1. Jen-Cheng Huang, Joo Hwan Lee, Hyesoon Kim, and Hsien-Hsin S. Lee. "GPUMech: GPU Performance Modeling Technique Based on Interval Analysis." In *Proceedings of the 47th IEEE/ACM International Symposium on Microarchitecture (MICRO-47)*, pp.268-279, Cambridge, England, December, 2014.

GP2. Jen-Cheng Huang, Lifeng Nai, Hyesoon Kim, and Hsien-Hsin S. Lee. "TBPoint: Reducing Simulation Time for Large Scale GPGPU Kernels." In *Proceedings of the 28th International Parallel and Distributed Processing Symposium (IPDPS)*, pp.437-446, Phoenix, AZ, 2014.

GP3. Hong Jun Choi, Dong Oh Son, Seung Gu Kang, Jong Myon Kim, Hsien-Hsin S. Lee, and Cheol Hong Kim. "An Efficient Scheduling Scheme Using Estimated Execution Time for Heterogeneous Computing Systems." In *Journal of Supercomputing*, 65(2), pp.886-902, 2013.

GP4. Abderrahim Benquassmi, Eric Fontaine, and Hsien-Hsin S. Lee. "Parallelization of Katsevich CT Image Reconstruction Algorithm on Generic Multi-Core Processors and GPGPU." In *GPU Computing GEMS, Section 10 Medical Imaging, Chapter 31*, Wen-Mei Hwu (editor-in-chief), pp.659-677, Morgan Kaufmann Publishers, 2011.

GP5. Dong Hyuk Woo and Hsien-Hsin S. Lee. "COMPASS: A Programmable Data Prefetcher Using Idle GPU Shaders." In *Proceedings of the 16th IEEE International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XV)*, pp.297-309, Pittsburgh, PA, March, 2010. (Acceptance rate = 17.7%, 32/181)

GP6. Ahmad Sharif and Hsien-Hsin S. Lee. "Total Recall: A Debugging Framework for GPUs." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware (GH-08)*, pp.13-20, Sarajevo, Bosnia-Herzegovina, June, 2008.

GP7. Eric Fontaine and Hsien-Hsin S. Lee, "Optimizing Katsevich Image Reconstruction Algorithm on Multicore Processors." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

GP8. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee, "POD: A Parallel On-Die Architecture." In *Proceedings of the 11th Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, Massachusetts, September, 2007. (**Award Session**)

GP9. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, and Hsien-Hsin S. Lee. "Chameleon: Virtualizing Idle Acceleration Cores of A Heterogeneous Multi-Core Processor for Caching and Prefetching." In *ACM Transactions on Architecture and Code Optimization*, vol.7, no.1, pp.1-35, April, 2010.

Energy Efficient Design

EE1. Mrinmoy Ghosh, Simon Ford, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. "Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED-09)*, pp.165-170, San Francisco, CA, August, 2009. (**Selected as one of seven papers of ISLPED highlight for publicity and press.**)

EE2. Hrishikesh Amur, Ripal Nathuji, Mrinmoy Ghosh, Karsten Schwan, and Hsien-Hsin S. Lee. "IdlePower: Application-Aware Management of Processor Idle States." In *Workshop on Managed Many-Core Systems (MMCS) co-located with ACM/IEEE International Symposium on High Performance Distributed Computing (HPDC)*, Boston, MA, June, 2008.

EE3. Chinnakrishnan S. Ballapuram, Ahmad Sharif, and Hsien-Hsin S. Lee, "Exploiting Access Semantics and Program Behavior to Reduce Snoop Power in Chip Multiprocessors." In *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII)*, pp.60-69, Seattle, WA, 2008. (acceptance rate = 31/127, 24.4%)

EE4. Chinnakrishnan S. Ballapuram and Hsien-Hsin S. Lee, "Improving TLB Energy for Java Applications on JVM." In *Proceedings of the International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII)*, pp.218-223, Samos, Greece, 2008.

EE5. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Virtual Exclusion: An Architectural Approach to Reducing Leakage Energy in Caches for Multiprocessor Systems." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

EE6. Dong Hyuk Woo, Mrinmoy Ghosh, Emre Ozer, Stuart Biles and Hsien-Hsin S. Lee, "Reducing Energy of Virtual Cache Synonym Lookup using Blooming Filters." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.179-189, Seoul, Korea, October, 2006. (Regular paper acceptance rate = 24.3%, 25/103)

EE7. Chinnakrishnan S. Ballapuram, Kiran Puttaswamy, Gabriel H. Loh and Hsien-Hsin S. Lee, "Entropy-based Low Power Data TLB Design." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.304-311, Seoul, Korea, October, 2006. (Short paper acceptance rate = 39.8%, 41/103)

EE8. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "DRAMdecay: Using Decay Counters to Reduce Energy Consumption in DRAMs." In *Proceedings of the 3rd Watson Conference on Interaction between Architecture, Circuits and Compilers (PAC^2)*, Yorktown Heights, NY, October, 2006.

EE9. Mrinmoy Ghosh, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee, "Efficient System-on-Chip Energy Management with a Segmented Bloom Filter." In *Proceedings of the Architecture of Computing Systems*

(ARCS'05), pp.283-297, Frankfurt, Germany, March 2006. (acceptance rate = 21%)

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